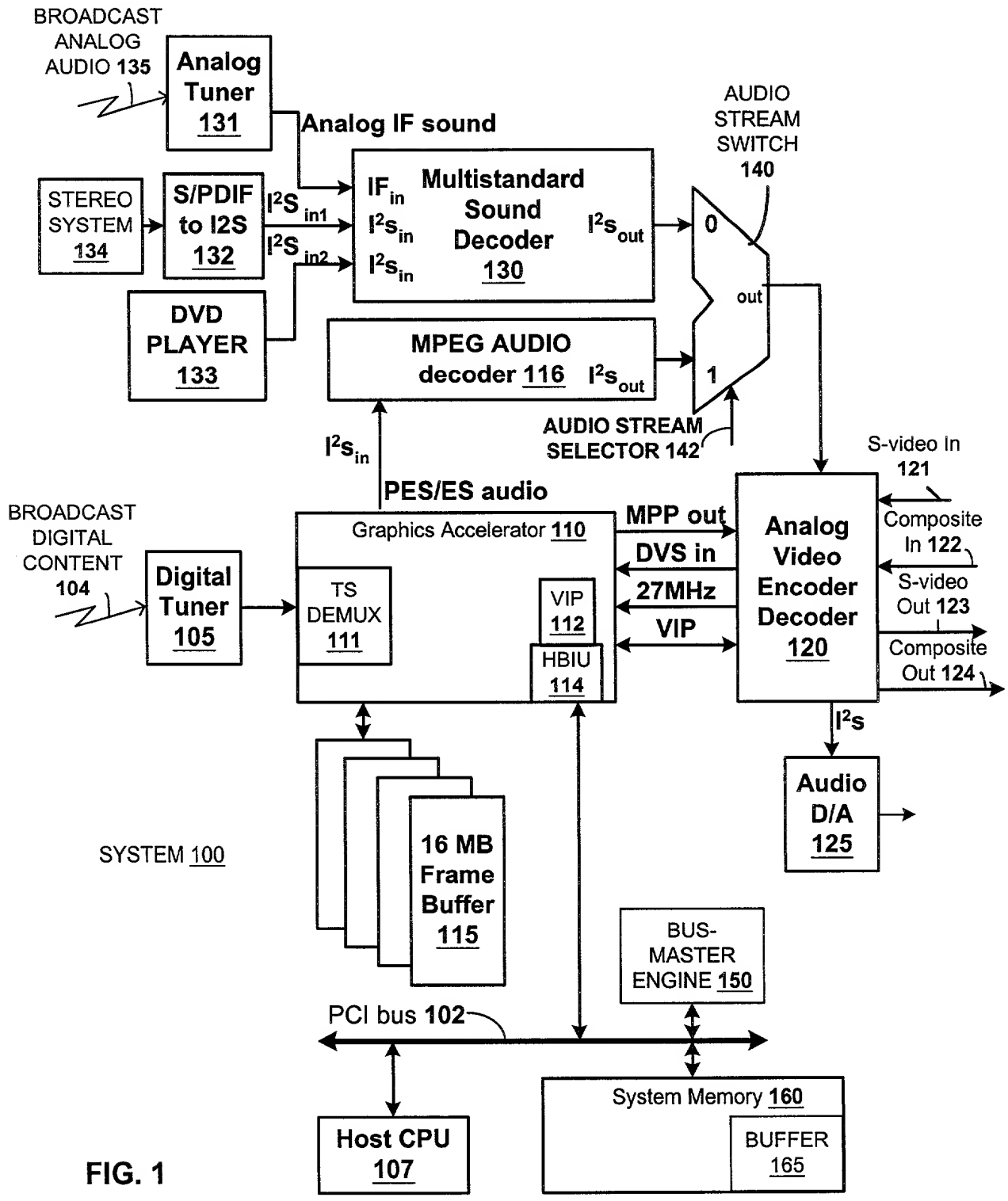
BROADCAST ANALOG AUDIO 135
Analog Tuner 131
Analog IF sound
AUDIO STREAM SWITCH 140
STEREO SYSTEM 134
S/PDIF to I2S 132
I2S in1
I2S in2
IFin
I2sin
I2sin
Multistandard Sound Decoder 130
I2sout
0
out
1
DVD PLAYER 133
MPEG AUDIO decoder 116
I2sout
AUDIO STREAM SELECTOR 142
I2sin
PES/ES audio
S-video In 121
BROADCAST DIGITAL CONTENT 104
Digital Tuner 105
Graphics Accelerator 110
MPP out
DVS in
27MHz
VIP
Analog Video Encoder Decoder 120
Composite In 122
S-video Out 123
Composite Out 124
TS DEMUX 111
VIP 112
HBIU 114
I2s
Audio D/A 125
16 MB Frame Buffer 115
SYSTEM 100
BUS-MASTER ENGINE 150
PCI bus 102
System Memory 160
BUFFER 165
Host CPU 107

FIG. 1

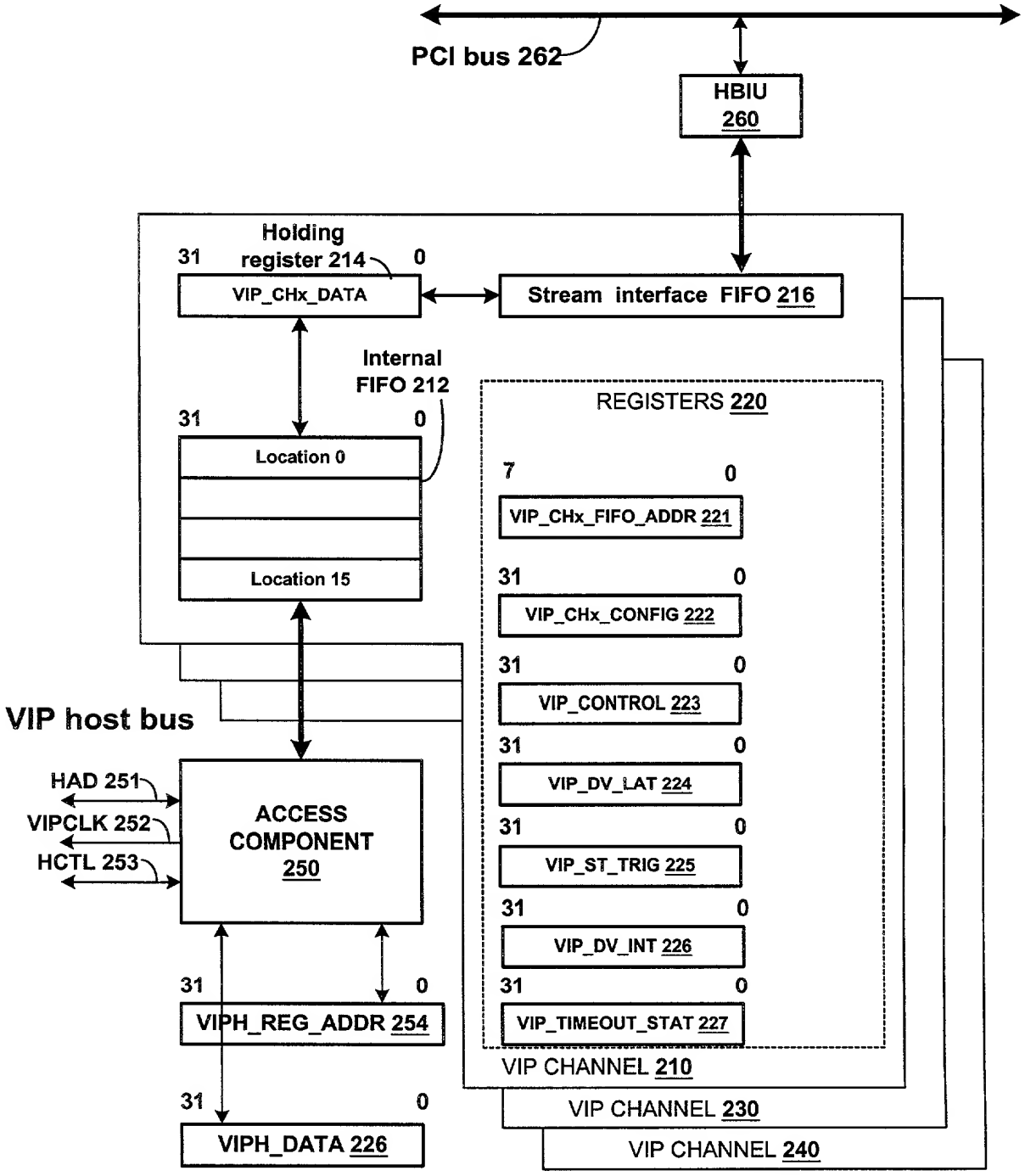
PCI bus 262
HBIU
260
Holding
register 214
31
0
VIP_CHx_DATA
Stream interface FIFO 216
Internal
FIFO 212
31
0
Location 0
Location 15
REGISTERS 220
7
0
VIP_CHx_FIFO_ADDR 221
31
0
VIP_CHx_CONFIG 222
31
0
VIP_CONTROL 223
31
0
VIP_DV_LAT 224
31
0
VIP_ST_TRIG 225
31
0
VIP_DV_INT 226
31
0
VIP_TIMEOUT_STAT 227
VIP host bus
HAD 251
VIPCLK 252
HCTL 253
ACCESS
COMPONENT
250
31
0
VIPH_REG_ADDR 254
31
0
VIPH_DATA 226
VIP CHANNEL 210
VIP CHANNEL 230
VIP CHANNEL 240

FIG. 2

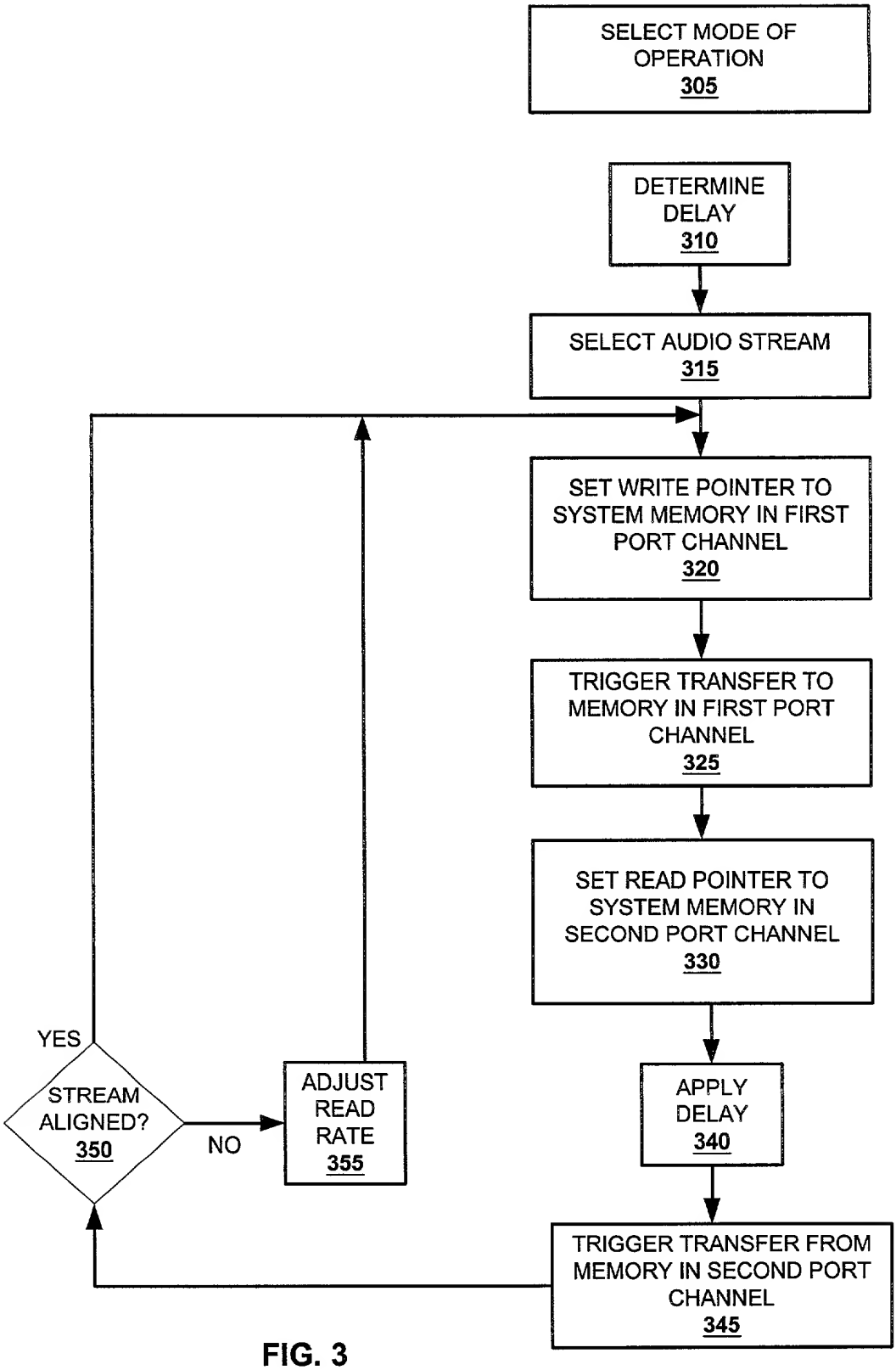
SELECT MODE OF OPERATION
305
DETERMINE DELAY
310
SELECT AUDIO STREAM
315
SET WRITE POINTER TO SYSTEM MEMORY IN FIRST PORT CHANNEL
320
TRIGGER TRANSFER TO MEMORY IN FIRST PORT CHANNEL
325
SET READ POINTER TO SYSTEM MEMORY IN SECOND PORT CHANNEL
330
APPLY DELAY
340
TRIGGER TRANSFER FROM MEMORY IN SECOND PORT CHANNEL
345
STREAM ALIGNED?
350
YES
NO
ADJUST READ RATE
355

FIG. 3

VIPH_CONTROL - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_CLK_SEL	3:0	0x0	VIPCLK is derived from internal memory clock (XCLK) VIPH_CLK_SEL specifies the clock-divide down from XCLK to VIPCLK.
VIPH_SWAP0_HOST	4	0x0	Data from host is byte-swapped when 1. Data from host is not swapped when 0. This applies to port0.
VIPH_SWAP1_HOST	5	0x0	Data from host is byte-swapped when 1. Data from host is not swapped when 0. This applies to port1.
VIPH_SWAP2_HOST	6	0x0	Data from host is byte-swapped when 1. Data from host is not swapped when 0. This applies to port2.
VIPH_SWAP0_RIP	8	0x0	Data from VIP-slave is byte-swapped when 1. Data from VIP-slave is not swapped when 0. This applies to port0.
VIPH_SWAP1_RIP	9	0x0	Data from VIP-slave (ripper) is byte-swapped when 1. Data from VIP-slave (ripper) is not swapped when 0. This applies to port.
VIPH_SWAP2_RIP	10	0x0	Data from VIP-slave (ripper) is byte-swapped when 1. Data from VIP-slave (ripper) is not swapped when 0. This applies to port2.
VIPH_MAX_WAIT	15:12	0x0	Setting this field to zero implies no time-out detection. VIP master waits for a maximum of 16 VIP phases before issuing time-out.
VIPH_CH0_CHUNK	18:16	0x0	Chunk transfer size between VIP and stream interface block for port 0.
VIPH_CH1_CHUNK	22:20	0x0	Chunk transfer size between VIP and stream interface block for port 1.
VIPH_CH2_CHUNK	26:24	0x0	Chunk transfer size between VIP and stream interface block for port 2.
VIPH_EN	29	0x0	0 = VIP turned off. 1 = VIP on.
VIPH_VIPCLK_DIS	30	0x0	0 = VIPCLK is running. 1 = stops the VIPCLK to save power.
VIPH_REG_RDY (R)	31	0x0	To insure that VIP register reads does not overlap due to VIP bus delays, this bit is used to synchronize VIP register reads. Submit new register read when 1, and don't submit when 0.

FIG. 4

VIPH_DV_LAT - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_TIME_UNIT	11:0	0x0	Basic time slice
VIPH_DV0_LAT	19:16	0x0	Specifies how many time slices port 0 gets.
VIPH_DV1_LAT	23:20	0x0	Specifies how many time slices port 1 gets.
VIPH_DV2_LAT	27:24	0x0	Specifies how many time slices port 2 gets.
VIPH_ST_TRIG - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_ST0_START	0	0x0	trigger data streaming through port0 when this bit is set high To stop the streaming, VIPH_ST0_STOP must be set low, and then follow by setting this bit low.
VIPH_ST1_START	1	0x0	trigger data streaming through port1 when this bit is set high To stop streaming, set VIPH_ST1_STOP to high, and then follow by setting this bit low.
VIPH_ST2_START	2	0x0	trigger data streaming through port2 when this bit is set high To stop the data streaming, set VIPH_ST2_STOP to high, and then follow by setting this bit low.
VIPH_ST0_STOP	4	0x0	To stop data streaming on port0, set this bit high before VIPH_ST0_START is set low. Terminating chip-to-system data streaming will result in some data getting flushed out of pipeline. But terminating system-to-chip data streaming will not cause a flush as all the data in the pipeline will be eventually drained out to the VIP slave.
VIPH_ST1_STOP	5	0x0	To stop data streaming through port 1, set this bit high.
VIPH_ST2_STOP	6	0x0	To stop data streaming through port 2, set this bit high.

FIG. 5

VIPH_DV_INT - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_DV0_INT_EN	0	0x0	0 = no interrupt polling through device0 1 = poll interrupt through device0
VIPH_DV1_INT_EN	1	0x0	0 = no interrupt polling through device1 1 = interrupt polling through device1
VIPH_DV2_INT_EN	2	0x0	0 = no interrupt polling through device2 1 = interrupt polling through device2
VIPH_DV0_INT (R)	4	0x0	status of interrupt from device0
VIPH_DV0_AK (W)	4	0x0	clear device0 interrupt with a '1'
VIPH_DV1_INT (R)	5	0x0	status of interrupt from device1
VIPH_DV1_AK (W)	5	0x0	clear device1 interrupt with a '1'
VIPH_DV2_INT (R)	6	0x0	status of interrupt from device2
VIPH_DV2_AK (W)	6	0x0	clear device2 interrupt with a '1'
GEN_INT_CNTL - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_INT_EN	24	0x0	0=Disable 1=Enable
CHIP_INT_EN	25	0x0	Enable chip interrupt. 0=Disable 1=Enable
GEN_INT_STATUS - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_INT (R)	24	0x0	0=No event 1=Event has occurred, interrupting if enabled
CHIP_INT (R)	25	0x0	Chip interrupt 0=No event 1=Event has occurred, interrupting if enabled

FIG. 6

VIPH_TIMEOUT_STAT - RW - 32 bits -			
Field Name	Bits	Default	Description
VIPH_FIFO0_STAT (R)	0	0x0	0 = port0 is fine and working. 1 = port0 time-out or hung.
VIPH_FIFO0_AK (W)	0	0x0	clear FIFO0_STAT with a '1'
VIPH_FIFO1_STAT (R)	1	0x0	0 = port1 is fine and working. 1 = port1 time-out or hung.
VIPH_FIFO1_AK (W)	1	0x0	clear FIFO1_STAT with a '1'
VIPH_FIFO2_STAT (R)	2	0x0	0 = port2 is fine and working. 1 = port2 time-out or hung.
VIPH_FIFO2_AK (W)	2	0x0	clear FIFO2_STAT with a '1'
VIPH_REG_STAT (R)	4	0x0	0 = register port is fine and working. 1 = register port time-out or hung.
VIPH_REG_AK (W)	4	0x0	clear REG_STAT with a '1'
VIPH_AUTO_INT_STAT (R)	5	0x0	0 = auto interrupt is fine and working. 1 = auto interrupt time-out or hung.
VIPH_AUTO_INT_AK (W)	5	0x0	clear AUTO_INT_STAT with a '1'
VIPH_FIFO0_MASK	8	0x0	0 = does not enable system interrupt on port0. 1 = enable system interrupt on port0.
VIPH_FIFO1_MASK	9	0x0	0 = does not enable system interrupt on port1. 1 = enable system interrupt on port1.
VIPH_FIFO2_MASK	10	0x0	0 = does not enable system interrupt on port2. 1 = enable system interrupt on port2.
VIPH_REG_MASK	12	0x0	0 = does not enable system interrupt. 1 = enables system interrupt.
VIPH_AUTO_INT_MASK	13	0x0	
VIPH_DV0_INT_MASK	16	0x0	
VIPH_DV1_INT_MASK	17	0x0	
VIPH_DV2_INT_MASK	18	0x0	
VIPH_INTPIN_EN	20	0x0	0 = no physical pin used for VIP interrupt. 1 = physical pin used for VIP interrupt.
VIPH_REGR_DIS	24	0x0	0 = any host read from VIPH_REG_DATA will trigger VIP register cycle. 1 = reading from VIPH_REG_DATA will not trigger VIP register cycle.

FIG. 7

VIPH_CHX_DATA - RW - 32 bits, X=0,1,2 -			
Field Name	**Bits**	**Default**	**Description**
VIPH_CHX_DATA	31:0	0x0	Those 3 registers are symbolic only. They do not exist. But their locations are used as destination / source address for VIP ports 0,1 and 3 and allow connection to stream interface block for transfer to / from system memory and VIP port.
VIPH_CHX_ADDR - RW - 32 bits, X=0,1,2 -			
Field Name	**Bits**	**Default**	**Description**
VIPH_CHX_FIFO_ADDR	7:0	0x0	VIP command byte for port X (X=0,1,2) –1s byte of transfer. Selecting 1 of 16 FIFO ports (status 0, status 1, FIFO A,B,C or user defined FIFOs). bit[3:0] = FIFO address range. bit[4] = register access when 0 and FIFO access when 1 bit[5] = register write when 0 and register read when 1 bit[7:6] = slave device id
VIPH_REG_ADDR - RW - 32 bits -			
Field Name	**Bits**	**Default**	**Description**
VIPH_REG_AD	15:0	0x0	VIP Address + Command Phase for VIP register access. bit[11:0] : slave register address range bit[12] : 0 = register access 1 = FIFO access bit[13] : 0 = register write 1 = register read bit[15:14]: slave device id
VIPH_REG_DATA - RW - 32 bits -			
Field Name	**Bits**	**Default**	**Description**
VIPH_REG_DT	31:0	0x0	VIP data for register access (4 bytes in burst).

FIG. 8